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Fabrication of the voltage-controlled semiconductor capacitors: some new insights

Voltage-controlled semiconductor capacitors (VCSC) of original design have been first described in [1,2]. As compared to other known semiconductor devices our VCSC allow to handle the unprecedented levels of high- and ultrahigh frequency signal power when used in parametric generators and converters. In addition, VCSC can be used as power transformers and very fast varactors with extremely large tuning range.

The present paper considers the problems of fabrication of voltage-controlled semiconductor capacitors. Experimental data are presented, as well as the results of simulations, which provide some very useful insights into physics and technology of VCSC and pave the way to better device design.

1. Fabrication of voltage-controlled semiconductor capacitors

We fabricated the device shown schematically in Fig.1. The main body of the device consists of p-base (with an area 0.6-1.0 mm^2) having laterally nonuniform doping so that the acceptor concentration decreases from left to right. The length (L) of p-base along x-coordinate varied from 10 to 50 μm. Two ohmic contacts are fabricated: contact 1to the active region and contact 2 for n^+-substrate. Gate oxide thickness was 0.2 μm. It was assumed that by increasing the reverse bias applied to p-n junction we could shrink in a controlled fashion the neutral region in the p-base along x-coordinate. Then, simultaneously with usual decrease of p-n junction depletion capacitance, we should observe a corresponding variation in VCSC (measured between the gate contact and contact 1).

For device fabrication six silicon wafers were used (n-type, heavily Sb-doped to a concentration of electrons 5×10^{19} cm^{-3} with 12 μm - thick epitaxial layer on top doped to 10^{15} cm^{-3} also n-type). In general, 12 different nonuniform p-type doping distributions along x-coordinate have been realized and tested in our work.

In order to obtain a nonuniform distribution of acceptor concentration along x-coordinate we have implemented the following approach. We perform a diffusion of acceptor impurity through the system of stripe openings in the masking oxide with a pre-calculated variable widths. In this way, we were able to achieve almost linear variation of acceptor concentration in p-base in lateral direction. The basic idea of our trick is explained in Fig.2. Acceptor impurity is introduced into a semiconductor through an array of variable-width openings in the masking layer (width $H_0(x)$, inter-window spacing being fixed at H-const) followed by usual thermal annealing. Initially the impurity concentration in semiconductor under the mask is zero whereas in the windows it is determined by the time of drive-in diffusion or ion dose during implantation. For annealing times $t\approx H^2/D_a$ (D_a is impurity diffusion coefficient) acceptor atoms will penetrate under the masked regions due to lateral diffusion from neighboring windows. For the average ion dose D(x) in the section of the device near the specific x-coordinate with opening width $H_0(x)$ ($H_{min}<H_0(x)<H_{max}$) we can write $D(x)\approx P(x)D_0$, where D_0 is implant dose and

$$P(x) = \frac{H_0(x)}{H_0(x) + H} \tag{1}$$

$H_0(x)$ being the x-dependent width of the window, the function P(x) may be called the local mask transparency because it is simply equal to the ratio of the open area to the sum of open and masked areas in the vicinity of a specific x-coordinate. Obviously, by varying the local mask transparency one should be able to create almost any desirable lateral impurity profile.

The final distribution of acceptor impurity in the base $N(\xi,x)$ can be easily estimated from a simple one-dimensional diffusion expression

$$N(\xi, x) \approx P(x) D_0 (\pi D_a t)^{-\frac{1}{2}} \exp(-\xi^2 / 4 D_a t) \tag{2}$$

where ξ is a depth under the surface. Fig.3 illustrates the resulting impurity profile for the mask with five openings having linearly decreasing (from H_0 to $0.2H_0$) window's width and fixed inter-window spacing ($H=H_0$). As can be seen from Fig.3 the time required to obtain a smooth impurity profile is about $H^2/0.25D_a$.Thus, using a standard diffusion through the system of variable-width openings in the masking layer we successfully solve the fabrication problem of controlled laterally nonuniform impurity distribution in semiconductor wafer.

In our experiments we used the boron doses (E= ?keV) from 1×10^{12} to 3×10^{12} ions per cm^2 , annealing times have been varied from 14 to 30 hours and maximum (minimum) window widths used were 7μm (2.8 μm). Using this approach we were able to fabricate a p-base in which the boron concentration increases almost linearly toward the ohmic contact from beneath the gate (contact number 1 in Fig.3).

2. The strange results of C-V measurements

The pre-calculated value of the punch-through reverse voltage (U_p) for p-base in our devices have been expected to be less than 5V in all cases:

$$U_p = \max\left\{\frac{q}{\varepsilon}\int_0^d N_i(x,y,z) z dz\right\} < 5V \tag{3}$$

We expected that by application of the reverse bias ($U>U_p$) to the p-n junction we can force the space-charge layer to fill the whole body of p-base region and then the minimal value of VCSC should be about 4-6 pF (depending on the specific device geometry). But experimental C-V measurements indicate that full depletion of p-base is never achieved for any reverse bias. Contrary to our expectations, a certain fraction (1/3-1/5) of the p-base material remains undepleted even at highest reverse bias used, see Fig.5. The ratio C_{min}/C_{max} was measured to be greater than 1/5, whereas the expected magnitude of this ratio should be less than 1/30. Moreover, the minimum value of VCSC was practically independent of the gate voltage.

2. Explanation of measured results and refinement of device structure

For the fabrication of varactors and voltage-controlled semiconductor capacitors with

a large tuning range (C_{min}/C_{max}) two questions naturally arise in view of experimental results outlined in the proceeding paragraph:

1. Why full depletion of mobile carriers in a p-base region of a device is not achieved?
2. What should be done in order to obtain the necessary full depletion?

To answer the first question a 2D simulation of our device was undertaken. Within standard drift-diffusion model the following problem has been formulated and solved (cf.Fig.6):

$$\nabla^2\varphi = -\frac{q}{\varepsilon}(N_d - N_a + p - n) \tag{4}$$

$$J_n = -q\mu_n\nabla\varphi + q\nabla D_n n \tag{5}$$

$$J_p = -q\mu_p\nabla\varphi - q\nabla D_p p \tag{6}$$

$$\frac{dn}{dt} = 0 = -U + \frac{1}{q}\nabla J_n \tag{7}$$

$$\frac{dp}{dt} = 0 = -U + \frac{1}{q}\nabla J_p \tag{8}$$

$$U = \frac{np - n_i^2}{\tau_n(p + n_i) + \tau_p(n + n_i)} \tag{9}$$

We used the following boundary conditions:

on the first upper ohmic contact (cf. Fig.6)

$$\varphi = \varphi_1;\ \ p = p_1;\ \ n = n_1;\ \ pn = n_i^2;\ \ n - p = N_d - N_a; \tag{10}$$

on the second ohmic contact, i.e. at the bottom and right-hand boundary of simulation domain (cf. Fig.6)

$$\varphi = 0;\ \ pn = n_i^2;\ \ p = p_1\exp(-\frac{q\varphi_s}{kT});\ \ \ n = n_1\exp(\frac{q\varphi_s}{kT}) \tag{11}$$

at the semiconductor-insulator interface the normal component of electron and hole current density is identically zero (cf. Fig.6), hence

$$J_{p_y} = 0;\ \ J_{n_y} = 0;\ \ \frac{d\varphi}{dy} = const = 0 \tag{12}$$

at the left-hand boundary due to symmetry

$$\frac{d\varphi}{dx} = 0;\ \ \ \frac{dn}{dx} = 0;\ \ \frac{dp}{dx} = 0 \tag{13}$$

In the expressions above the usual symbols have been used: φ is potential, $J_n(J_p)$ is electron (hole) current density, $\mu_n(\mu_p)$ is electron (hole) mobility, $D_n(D_p)$ is electron (hole) diffusion coefficient, p(n) is hole(electron) concentration, q is an elementary charge, N_d-N_a is net doping concentration, ε is dielectric constant of Si, φ_s is a built-in barrier potential, n_i is intrinsic carrier concentration and $\tau_n(\tau_p)$ is electron (hole) lifetime (relaxation time). We used empirical relations $\mu_{n,p}=F(E, N_d-N_a)$ [3] where E is electric field and Einstein relation

$$\frac{\mu_{n,p}kT}{q} = D_{n,p} \qquad (14)$$

in our calculations.

Fig.6 illustrates the solution obtained on a grid with equal space steps along x and y axis (5.0×10^{-8} m), $n_i=1.5\times10^{10}$ cm^{-3}, for p-base with doping concentration of 2×10^{15} cm^{-3}, upper contact width 0.5μm, φ_s=0.8V, and $\tau_n=\tau_p=10^{-8}$ s. Equipotential lines in Fig.6 correspond to the applied voltage of 8V ($U=\varphi_1-\varphi_2$= - 8V). Note that isopotential line for φ= -7.9 V approximately defines the boundary of the neutral region beyond which the potential changes insignificantly. It is clearly seen from Fig.6 that near the SiO_2/Si interface a neutral layer exists even for the reverse bias (U) twice as large as a punch-through voltage (U_p). An important conclusion can be drawn from this observation: the absence of the full depletion in p-base is not caused by faulty technological route. The true reason is that the lowest bias required for the full depletion of the SiO_2/Si interface is much larger than U_p. By extensive numerical work (using simply a trail-and error method) it was found that insertion of a thin n- or i-layer under the SiO_2 film rectifies the situation and allows to achieve full depletion for reverse biases $U\geq U_p$. This is illustrated by Fig.7 where equipotential lines are drawn for exactly the same conditions as in Fig.6 the only difference being that a layer of i-Si with $n\approx2\times10^{10}$ cm^{-3} and a thickness of 5×10^{-8}m was inserted beneath the SiO_2. To explain our finding in general terms let us consider Fig.8 where a semiconductor device is shown consisting of region (1)(which is chosen to be p-type) with a first ohmic contact (11) fabricated on the one part of the upper surface of the said region while on the remaining part of the surface an insulating layer (5) is formed with conductive contact (6) on it. On the bottom and (for simplicity) right-hand side of region (1) the Schottky contact (2) is fabricated with an ohmic contact (12) attached to it. To simplify the discussion it will be assumed that $N_i(x,y)=N_a-N_d$.

For the constant normal component of the electric field at semiconductor-insulator interface (E_y=const) which corresponds to the application of constant voltage (including zero) between ohmic contact (11) and gate contact (6), the Poisson equation near the interface

$$\frac{dE_x}{dx}+\frac{dE_y}{dy}=\frac{q}{\varepsilon}\left[p+n-N_i(x,y)\right] \qquad (15)$$

is simplified, and takes the form

$$\frac{dE_x}{dx} = \frac{q}{\varepsilon}[\, p + n - N_i(x,y)] \tag{16}$$

Since $E_x = -\frac{d\varphi}{dx}$ and for the fully depleted p-region (1) we have n,p<<N_i(x,y), one obtains from (16) at the interface with an isolating layer

$$\frac{d^2\varphi}{dx^2} = \frac{q}{\varepsilon} N_i \tag{17}$$

for $y = d$ and $0 \le x \le L$, where φ is the potential and L is the extension of active p-region under the insulator in x-direction. Solving this equation under conditions of $\varphi(0,d) = 0$ and $\frac{d\varphi}{dx} = 0$ at $x = d$, we obtain

$$\varphi(x,d) = \frac{q}{\varepsilon}\int_0^x N_i(h,d)hdh; \quad \varphi(L,d) = \frac{q}{\varepsilon}\int_0^L N_i(h,d)hdh; \tag{18}$$

Here, $\varphi(L,d)$ is a minimal voltage drop between contacts (6) and (11) that guarantees the full surface depletion of mobile carriers in p-region at the interface with isolating layer. $\varphi(L,d)$ includes a built-in potential (φ_s), i.e. a potential drop in p-region in the absence of any external bias.

If $L >> d$ and, under depletion conditions, we obviously have that $N_i(x,y) >> n, p$, one can safely assume that potential is changing along y-coordinate much faster than along x-coordinate and, therefore, the Poisson equation (since $E_x = -\frac{d\varphi}{dx}$ and $E_y = -\frac{d\varphi}{dy}$) can be written as

$$\frac{d^2\varphi}{dy^2} = \frac{q}{\varepsilon} N_i(x,y) \tag{19}$$

with boundary conditions

$$\varphi(x,0) = 0; \quad \frac{d\varphi(x,y)}{dy} = 0 \tag{20}$$

The solution of (19) under conditions (20) can be found immediately

$$\varphi_1(x,y) = \frac{q}{\varepsilon}\int_0^y N_i(h,d)hdh; \quad \varphi_1(x,d) = \frac{q}{\varepsilon}\int_0^d N_i(h,d)hdh; \tag{21}$$

Here, $\varphi_1(x,d)$ is a minimal voltage between contacts (6) and (11) in Fig.8 when a depletion of p-region occurs in the bulk for x-section with $0 \le y \le d$. Obviously, $\varphi_1(x,d)$ includes a built-in potential φ_s at the semiconductor-insulator interface. Note that $\max\{\varphi_1(x,d)\} \equiv U_p$ - a punch-through reverse voltage for the full depletion of the bulk of p-region in x-section of the device.

Let U_i be the breakdown voltage on the p-base. Then for $U_p < U_i$ and $\varphi(L,d) < U_i$ the bias to be applied between contacts (6) and (11) in Fig.8 for the full depletion (bulk and interface) of the p-region (1) must fulfil the following requirements

$$U > U_p \quad \text{and} \quad U \ge \varphi(L,d) \tag{22}$$

Under these conditions the space-charge layer will extend to the whole volume of p-base region (1) in Fig.8. If than for the bias $\varphi(L,d) \ge U \ge U_i$ the space charge region of reverse – biased p-n junction fill the whole p-base except a thin layer underneath ohmic contact and a part of insulating layer which remains undepleted (see Fig.6 and Fig.8).

Now, if we provide a thin layer (3) under the insulating film and this layer: 1) will have an opposite conductivity type with respect to the main body (1) of the device, and 2) a thickness of the layer (3) will be only a fraction of the screening length, then, obviously, the surface of this layer in contact with an insulator will be depleted of mobile carriers from the very beginning. This simple fact explains the results of more elaborate 2D-simulations, as well as the results of C-V measurements presented in fig.9. Shown in this figure are experimental measurements of p-n junction capacitance and voltage-controlled capacitance (between ohmic contact to the region (1) and gate metallization) for devices *without* (curve A) and *with* (curve B) n-type layer beneath SiO_2. The n-type layer under gate oxide was fabricated by phosphorus ion implantation (E=70keV, $D=1.5\times10^{11}cm^{-2}$) before thermal oxidation. With n-layer in place, the calculated value of VCSC is in satisfying accordance with measured results.

4. Practical recommendations

One of the major advantages of the newly developed voltage-controlled semiconductor capacitor is that, in contrast to other known (at least, to me) semiconductor devices, VCSC is almost completely free of so called “electronic constraint” on the useful power level that can be taken from a given device. It is well known, that electrical breakdown puts a fundamental limit to the maximal voltage, which can be applied to the device. The second limitation removed in our VCSC is the size of the active region, which ultimately determines the high-frequency behavior of any known semiconductor device and is a major reason for aggressive deep submicron scaling in current VLSI. Our VCSC can deliver very high power levels in a microwave region when used as parametric frequency converters, generators or amplifiers.

It is, however, also true that in order to realize these advantages, one must have in mind that in parallel with VCSC at least two parasitic capacitances are always present: the p-n junction capacitance and gate-substrates capacitance.

The simplest equivalent circuit for VCSC-device is shown in fig.10. Here, U_c designates the voltage on VCSC (between gate metallization and ohmic contact to p-base), C_{pn} – capacitance of p-n junction between n-substrate and p-base. C_{gn} – capacitance between gate and n-substrate, and C_{pg} – the voltage-controlled capacitance. Since the part of external

voltage applied to p-n junction must always be less then breakdown voltage, we can write

$$\frac{U_c}{1+\frac{C_{pn}}{C_{pg}}} < U_i \tag{23}$$

Moreover, if a good decoupling is required between input (contracts to p-n junction) and output (contacts to p-base and gate) of the device, the potential drop on p-n junction should be much less than capacitance-controlling voltage:

$$\frac{U_c}{1+\frac{C_{pn}}{C_{pg}}} << U \tag{24}$$

This can be done in two ways: either by incorporating an additional capacitance in parallel with p-n junction, or by increasing the insulator layer thickness. A combination of these methods can also be used.

Thick insulating layers have large breakdown voltage and therefore permit to apply and extract a large power from VCSC. The fabrication of thick (d>10μm) isolating films is not a trivial problem for planar technology (the only exception consist in using of highly resistive (i-type) substrates). But very thick insulating (or semi-insulating) layers lead to unacceptable decrease in tuning range and for semi-insulating substrate there is a problem of using wafers less than 100-150 μm in thickness which is generally incompatible with existing technology due to the their low mechanical strength. Moreover, in order to reduce the spreading resistance and to rise the device Q-factor, it is reasonable to fabricate the ohmic contact to the active region in a grid-form. Fig.11 represents the VCSC device construction where the grid-like ohmic contact to n-type layer is fabricated (period *a*, metal stripe width a_1) with an insulating layer on top. Near the SiO_2/Si interface for the reason described above a thin p-type layer must be present (not shown in fig.11). The isolating layer is made separately and is simply pressed to the main device, which can be fabricated using standard planar technology.

In this device the tuning range (C_{max}/C_{min}) is reduced for thick i-layer. Let us calculate the C_{min}. In the literature [4] one can find the solution for analogous problem expressed through the elliptical functions, but the results obtained or their approximations expressible through the elementary functions [5], are not reproduced here, since application of these bulky formulas to the case in hand is too lengthy and , in fact, unnecessary. Our solution given below is much shorter and, at the same time, is sufficiently accurate for engineering estimates.

For $H_d >> a >> a_1$ (where H_d is the dielectric layer thickness) the potential in the arbitrary z-plane cross section of the insulator is a sum of the grid potential (with a period "a" along x-coordinate) and potential of the top-most electrode. It can be written as

$$\varphi = A\cos\left(\frac{x}{2\pi a}\right)\exp\left(-\frac{z}{2\pi a}\right)+\frac{\delta}{\varepsilon}(z-H_d) \tag{25}$$

The first term in this expression describes the periodic potential originated from the grid, whereas the second term pertains to the potential induced by top electrode. By direct substitution on can confirm that (25) is a solution of the Laplace equation. In (25) δ is the

surface charge density, ε is the dielectric constant of the isolating layer, A – constant, a – grid period, a_1 – the width of grid line. A and δ are determined from boundary conditions. If $a<<H_d$ the first term is vanishingly small and φ=0 for $z=H_d$. When z=0 and $\cos\left(\frac{x}{2\pi a}\right)=-1$ we have for the potential of the contact

$$\varphi = A + H_d \frac{\delta}{\varepsilon} \tag{26}$$

Periodic contact arrangement corresponds to an extremum of (25) at z=0 because contact's potential is a constant and any function variation near its extremum can be safely neglected. Differentiating (25) by z at z=0 and $\cos\left(\frac{x}{2\pi a}\right)=-1$ and taking into account that potential near grid is a sum of grid potential = $\frac{1}{2}\frac{a}{a_1}\frac{\delta}{\varepsilon}$ and the top electrode potential = $\frac{1}{2}\frac{\delta}{\varepsilon}$ one obtains

$$\frac{A}{2\pi a}+\frac{\delta}{\varepsilon}=\frac{1}{2}\frac{a}{a_1}\frac{\delta}{\varepsilon}+\frac{\delta}{2\varepsilon} \tag{27}$$

From this we have

$$A=\pi\left(\frac{a\delta}{a_1\varepsilon}+\frac{\delta}{2\varepsilon}-\frac{\delta}{\varepsilon}\right)=\pi a\frac{\delta}{\varepsilon}\left(\frac{a}{a_1}-1\right) \tag{28}$$

The tuning range $K = C_{\min}/C_{\max}$ is then given by

$$K=1+\frac{\pi a}{H_d}\left(\frac{a}{a_1}-1\right) \tag{29}$$

If, in parallel with p-n junction, a large capacitor is switched in, we can write

$$K=\frac{2}{1+\dfrac{1}{1+\dfrac{\pi a}{H_d}\left(\dfrac{a}{a_1}-1\right)}} \tag{30}$$

For this case Q-factor and maximal modulation coefficient m can be expressed as

$$Q\approx\frac{H_d d}{\varepsilon\rho\omega(a-a_1)};\qquad m_{\max}\approx\frac{1-K}{1+K}\approx\frac{\pi a}{2H_d}\left(\frac{a}{a_1}-1\right) \tag{31}$$

We conclude the article by presenting an example of estimation of the relevant device parameters for some selected specific application.

5. A worked example

Below an estimate is given for VCSC parameters to be used as a frequency converter from F_{min}= 1 GHz to F_{max} =5 GHz with 200 W peak power delivered (note, that if any of the existing varactors is used for the same purpose the power available will be *two orders of magnitude* lower).

Applied to the p-n junction is a signal with F_{max} -F_{min}=4 GHz, whereas to VSCS a signal with F_{min}=1 GHz is applied, and a tuned resonance circuit with a resonance frequency F_{max} + F_{min} is used. An estimation of the basic parameters of VCSC proceeds as follows:

1. Contact grid period must obey the obvious constraint

$$a < \frac{v_s}{F_{\max} + F_{\min}} = \frac{1\times10^5\, ms^{-1}}{5\times10^9\, s^{-1}} = 20\mu m \tag{32}$$

where v_s is the saturated drift electron velocity in Si (=1×10^5 ms^{-1}).

2. Let the insulating layer to be fabricated from quartz (with a breakdown electric field E $\approx 10^9 Vm^{-1}$) and let a thickness of this layer to be about 100 μm. Then,

$$K = \frac{2}{1+\dfrac{1}{1+\dfrac{\pi a}{H_d}\left(\dfrac{a}{a_1}-1\right)}} \approx 1.4 m_{\max} \approx \frac{1+K}{1-K} \approx 0.2 \tag{33}$$

3. The horizontal dimension of n-base (a_x) can be chosen from the condition

$$a_x = \frac{\lambda}{20} = \frac{c}{20F_{\max}\sqrt{\varepsilon}} \approx 1.5\ nm \tag{34}$$

the maximal capacitance being then

$$C_{\max} = \frac{2\varepsilon a_x^2}{H_d} \approx 1.5\times10^{-12} \quad \text{F} \tag{35}$$

4. The doping level of n-base can be varied in a wide range. Let us choose the thickness of n-base to be 1 μm with doping level of n=5×10^{15} cm^{-3}.
5. To find a maximum voltage to be applied to VCSC and a minimal value of the capacitance (C_P) to be switched in parallel with p-n junction, let us assume that a fraction of voltage, which drops on p-n junction, is 1 V. Then,

$$U_c = \frac{2PQ}{F_{\min}\sqrt{0.5C_{\max}}} \approx 1000 \quad \text{V} \tag{36}$$

and for Q=10, P=200 W one finally obtains

$$C_{\mathrm{P}} = \frac{0.5 C_{\max} \times U_c}{1\ V} = 7.5 \times 10^{-10} \quad \mathrm{F}$$

(37)

In this way, all relevant parameters of VCSC are now estimated. Fig.12 shows the calculated time dependence of the voltage on VCSC (with parameters given above) for different modulation coefficients (in the figure, E is the amplitude of the lower frequency signal and m is the modulation coefficient).

Acknowledgments

Without the financial support from V.I.Kolesnikov and A.S Lunev this work simply could not be done. The author wishes to express his sincere thanks to A.S Korenev, A.I.Maksutov, A.I Startsev and Yu.M.Fridman for their help during my work. The author is especially indebted to Dr. S.I.Chikichev who translated the manuscript into English.

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Figure captions

Fig1.Device structure.

Fig2.Diffusion mask configuration.

Fig3.Impurity profiles under the mask for different annealing times.

Fig4.Fragment of the mask used for the fabrication of laterally nonuniform impurity distributions in a p-base region of the device.

Fig5.Typical results of capacitance-voltage measurements.

Fig6.Equipotential lines in p-base for $U=2U_p$.

Fig7. Equipotential lines in p-base with i-layer inserted beneath the SiO_2 film (all other parameters being identical to that of fig.6).

Fig8. Illustrates why full depletion is impossible for device with a structure shown in fig.1.

Fig9. A comparison of the capacitance-voltage curves measured on VCSC:
A. Without n-layer under the gate;
B. With n-layer.

Fig10. A simplest equivalent scheme for the voltage-controlled semiconductor capacitor.

Fig11. VCSC with a thick insulating layer, which is simply pressed to the ohmic contact.

Fig12. The time dependence of the voltage on VCSC used as a frequency converter (from 1 GHz to 5 GHz) in a series circuit.

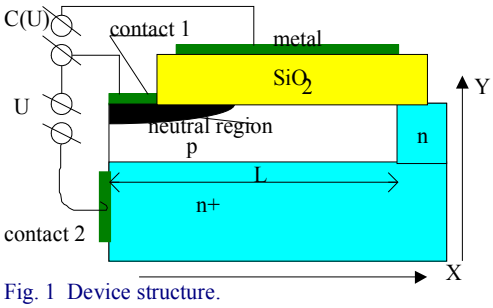

Fig. 1 Device structure.

Fig. 2. Diffusion mask configuration.

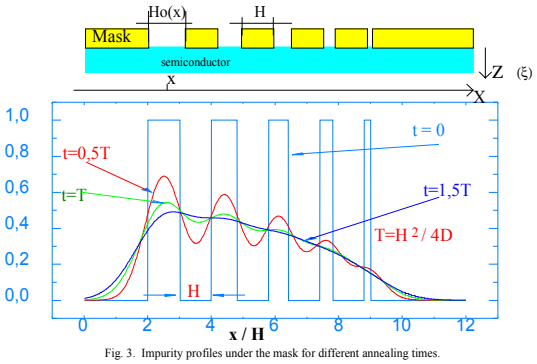

Fig. 3. Impurity profiles under the mask for different annealing times.

ξ

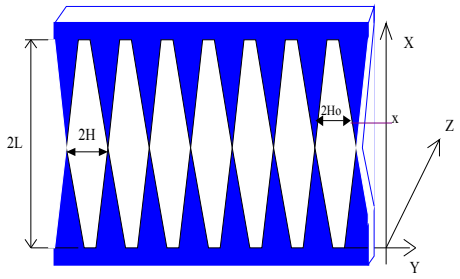

Fig.4. Fragment ofthe mask used for the fabrication of laterally nonuniform impurity distributions in the base region of the device.

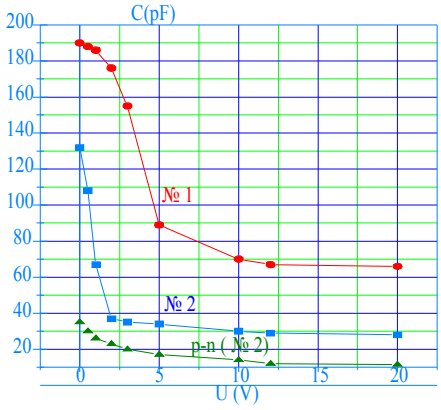

Fig. 5. Typical results of capacitancevoltage measurements.

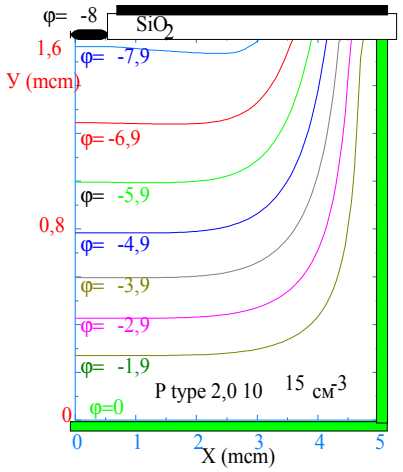

Fig. 6. Equipotential lines in p base for U=2U p

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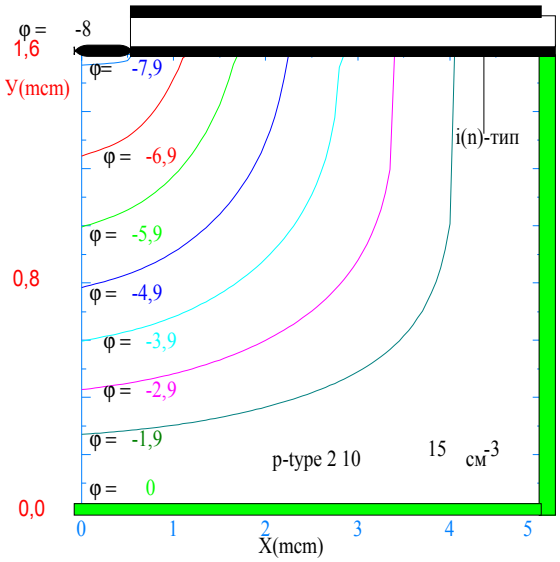


Fig. 7. Equipotential lines in p - base with i - layer inserted beneath the SiO_2 film (all other parameters being identical to that of fig.6).

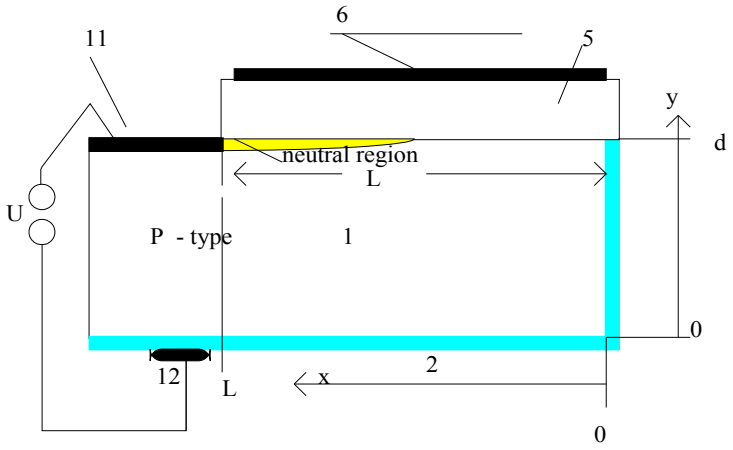
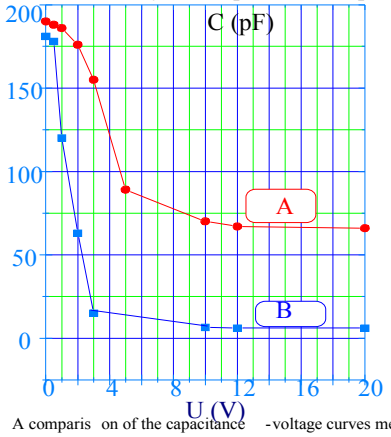


Fig.8. Illustrates why full depletion is impossible for device with a structure shown in fig.1



1- A comparis on of the capacitance -voltage curves measured on VCSC:

A. Without n - layer under the gate;
B. With n - layer.

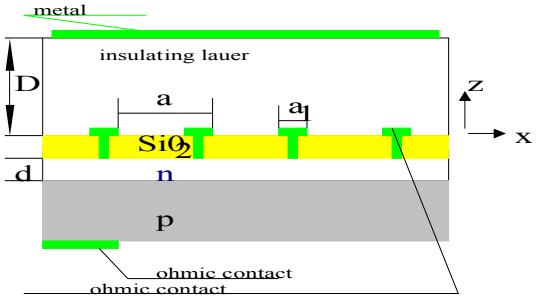
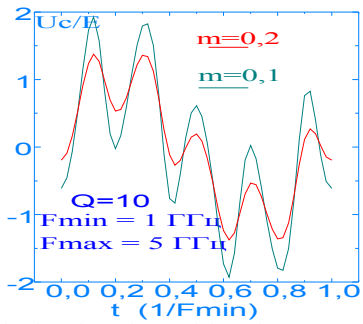


Fig. 11. VCSC with a thick insulating layer, which is simply pressed to the ohmic contact.



The time dependence of the voltage on VCSC used as a frequency con
(from 1 GHz to 5 GHz) in a series circuit.