APPENDIX 2

Voltage-controlled capacitors (capacitance transformers)

From a circuit designer's point of view any diode is no more than a non-linear resistor whereas a transistor is simply a voltage-controlled non-linear resistor – its output impedance is controlled by input signal. Quite similar to these trivial facts a voltage-controlled semiconductor capacitor is a device which output capacitance is controlled by a signal applied to the input. So, in contrast to varicap (or varactor) which has only two external leads, a voltage-controlled capacitor (VCC) is a three-(or more)-terminal device. Due to this special feature we envisioned that application field of VCC is vastly expanded in comparison with application field of traditional varicaps (in approximately the same ratio as application range of transistors exceeds that of diodes).

Voltage-controlled semiconductor capacitors (capacitance transformers) can be used for amplification and frequency transformation and are highly superior to transistors as concerns the useful power delivered to the external load since temperature constraints are greatly reduced (capacitors are heated only in proportion their Q-factor) and the so called electronic constraint, routed in breakdown voltage of any semiconductor junction (exactly this is a reason that power delivered by any semiconductor device is inversely proportional to the square of operating frequency) , is almost completely eliminated in our VCC. Voltage-controlled capacitors fit nicely into existing integrated circuit technology. Moreover, capacitance transformers are preferential against usual inductive transformers from technological and economic viewpoints and, we believe, could replace them at least in microwave frequency range.

VCC operational principle explained

Let us consider a voltage-controlled capacitor comprising a p-n junction with n-layer doped nonuniformely along x-coordinate (see Fig.1). On top surface of this p-n junction a dielectric layer is grown having a metallic electrode thereon. Both n and p regions are provided with ohmic contacts so that a reverse bias can be applied to the p-n junction. Let doping concentration in the n-layer $N_i(x,y)$ with $0 \le x \le x_{\max}$, $0 \le z \le F(x),$ and $y \le d,$ increases in some predetermined manner from $x_{\max}$ toward 0. Then, with increasing reverse bias the neutral (undepleted) region $H(U)$ would shrink and effective area of VCC electrodes (between neutral region and metallic overlayer 2) would also decrease. Thus, we see that concurrently with usual drop of p-n junction depletion capacitance to which bias is applied, another capacitance changes – that between undepleted part of n-layer under dielectric and metal film 2. It exactly this capacitance which we call VCC. If $C(t)$ is time dependence of VCC, $Q(T)$ is the charge on VCC electrodes, then voltage on VCC will be given by

$$V_2(t) = \frac{Q(t)}{C(t)}$$

Several examples are given below to illustrate the circuit use of VCC.

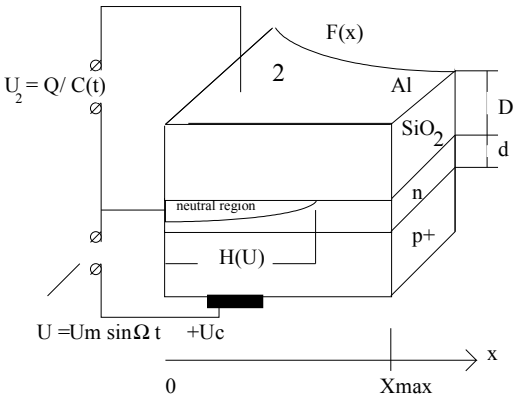


Fig. 1. The condenser, controlled by a voltage

Example 1. *Capacitance transformer with DC voltage supply and a diode*

Referring to Fig.1.1 one can see that applying a reverse bias pulse to the p-n junction we can decrease the VCC (a capacitance between n-layer and top-most metal film) thus forcing the voltage on VCC to increase. As a result the diode will be blocked and the VCC would discharge through the load resistance R_n. The maximum voltage on VCC is given by

$$U_c \approx E\frac{C_{\max}}{C_{\min}}$$

where E is the magnitude of supply voltage and $C_{\max}(C_{\min})$ is the maximal (minimal) value of VCC.

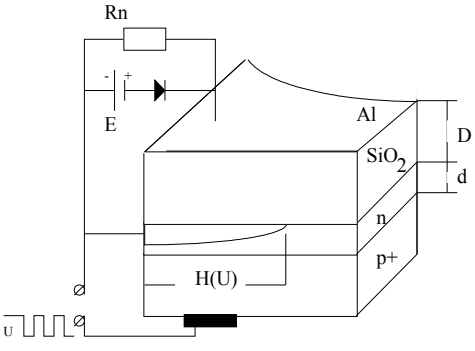
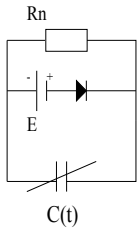


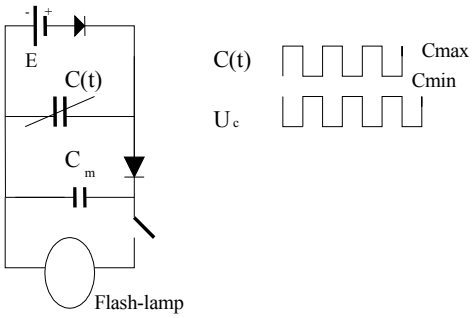
Fig 1.1 *Capacitance transformer with DC voltage supply and a diode*



The equivalent circuit.

Example 2. *Capacitance transformer with constant voltage source*

An example of application of capacitance transformer in the flash-lamp.



By application of the supply voltage pulses to semiconductor junction the voltage –controlled capacitance C (t) is also pulsed changing its magnitude abruptly from C_{min} to C_{max}. As a result the voltage on this capacitance varies from the value determined by dc voltage source E to E C_{max} /C_{min}. These pulses charge the main capacitor C_m to a voltage level of ~ E C_{max} /C_{min} (discharging through voltage source is blocked by the diode). The main capacitor discharges through the flash-lamp after closing the key.

In its turn, the main capacitor can be used as a voltage source enabling the voltage amplification of signals stage by stage in high-voltage transducers. This technical solution can be used when it is necessary to apply high voltages (including variable ones) to capacitive loads.

Similar device can be proposed as an alternative to existing ignition systems with inductive plugs for internal combustion engines.

Fig 2.1 shows capacitance transformer containing high constant voltage source E with a load resistor E, connected to n-layer and Al metallization of VCC. The input signal $0 \le z \le F(x),$ is applied to p-n junction. Under the influence of comparatively small input signal the VCC will be modulated, being a part of high voltage circuit. The calculated time dependence of VCC voltage is shown in Fig.2.2.

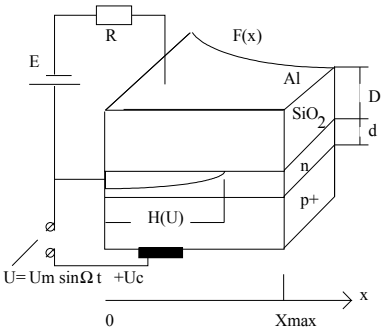


Fig 2.1. Capacitance transformer with constant voltage source

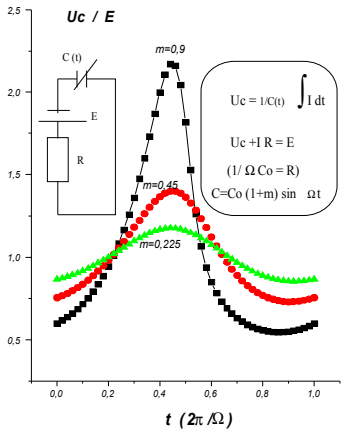


Fig. 2.2 **Voltage on controlled capacity**

Example 3. *A voltage-controlled capacitor with a predetermined C-V characteristic*

It goes without saying that ability to fabricate a device with a predetermined C-V characteristic opens the door to completely new dimension in circuit design. Below we show that our invention provides this unique opportunity.

Let us consider Fig.3.1 depicting a dielectric plate (for example, SiO_2) with metallized (2) bottom face. On the upper face of said insulating (or semi-insulating) wafer a set of conductive stripes (3) is formed. Over these stripes a p^+ - n junction is fabricated with laterally (along x-direction) non-uniform doping in the n-layer. The active device area containing conductive stripes is defined by $0 \le x \le x_{\max}$, $0 \le z \le F(x)$, and let the non-uniform doping profile $N_i(x,y)$ in the low-doped n-layer is such that impurity concentration increases from $x_{\max}$ toward 0. Then, by increasing the reverse bias applied to p^+-n junction we will force the space charge layer to fill gradually the volume of n-layer on the active area. The size of undepleted part of n-base will vary accordingly and effective area of VCC electrodes (between conductive stripes (3) and metallic film (2)) will be continuously decreased. To remove the undesirable capacitive coupling between metal layer (2) and p^+ -region the p-n junction (or Schottky barrier, as the case may be) can be fabricated upon only a small portion of conductive stripes. Now, choosing the *shape* $F(x)$ of the active region, we can achieve a predetermined C-V characteristic, which is given by the following equation

$$C(U) = C\min + \varepsilon_S / D \int_0^{H(U)} F(x)dx$$

where $C_{\min}$ is determined mainly by the size of the ohmic contact to n-layer.

Fig.3.2 illustrates the calculated shape of the active area of a particular VCC which when used in LCR-circuit will provide an ideal frequency modulator – for this purpose C-V characteristic must be of the type

$$C(U) = \frac{C_1}{(C_2 + U)^2}$$

It was assumed in the calculations that $\frac{C_{\max}}{C_{\min}} = 5$ and doping profile in the n-layer is linear so that $H(U) \sim x_{\max}\left(1 - \frac{U}{U_{\max}}\right)$.

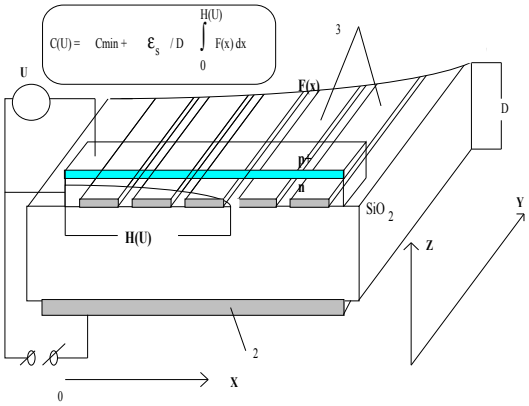


Fig.3.1 *A vo ltage - controlled capacitor with a predetermined C - V characteristic*

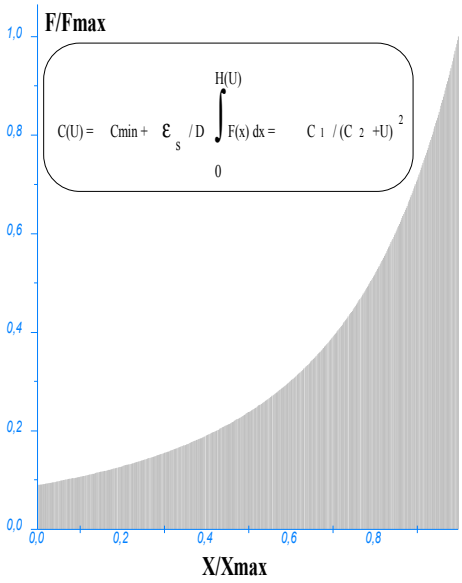


Fig. 3.2

Voltage-controlled capacitors described above can be used as active elements in high-power generators and mixers, since usual constraints imposed by breakdown voltage of thin space-charge layer in any semiconductor junction is removed in VCC as well as joule heating.

It is, however, also true that in order to realize these advantages, one must have in mind that in parallel with VCC at least two parasitic capacitances are always present: the p-n junction capacitance and gate-substrates capacitance.

The simplest equivalent circuit for VCC-device is shown in fig.4.1. Here, U_c designates the voltage on VCC (between gate metallization and ohmic contact to p-base), C_{pn} – capacitance of p-n junction between p^+-substrate and n-base. C_{pm} – capacitance between metal film and p+-substrate, and C_{nm} – the voltage-controlled capacitance. Since the part of external voltage applied to p-n junction must always be less then breakdown voltage, we can write $Uc/(1+ Cpn/ Cpm) < Ui$.

Moreover, if a good decoupling is required between input (contracts to p-n junction) and out- put (contacts to p-base and gate) of the device, the potential drop on p-n junction

should be much less than capacitance-controlling voltage: Uc/(1+ Cpn/ Cpm) < <U .

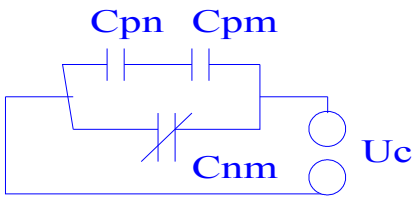


Fig.4.1 The simplest equivalent circuit fo

This can be done in two ways: either by incorporating an additional capacitance in parallel with p-n junction, or by increasing the insulator layer thickness. A combination of these methods can also be used.

Thick insulating layers have large breakdown voltage and therefore permit to apply and extract a large power from VCC. The fabrication of thick (d>10μm) isolating films is not a trivial problem for planar technology (the only exception consist in using of highly resistive (i-type) substrates). But very thick insulating (or semi-insulating) layers lead to unacceptable decrease in tuning range and for semi-insulating substrate there is a problem of using wafers less than 100-150 μm in thickness which is generally incompatible with existing technology due to the their low mechanical strength. Moreover, in order to reduce the spreading resistance and to rise the device Q-factor, it is reasonable to fabricate the ohmic contact to the active region in a grid-form. Fig.4.2 represents the VCC device construction where the grid-like ohmic contact to n-type layer is fabricated (period *a*, metal stripe width a_1) with an insulating layer on top. Near the SiO_2/Si interface a thin p-type layer must be present. The isolating layer is made separately and is simply pressed to the main device, which can be fabricated using standard planar technology. In this device the tuning range (C_{max}/C_{min}) is reduced for thick i-layer.(see Appendix 4).

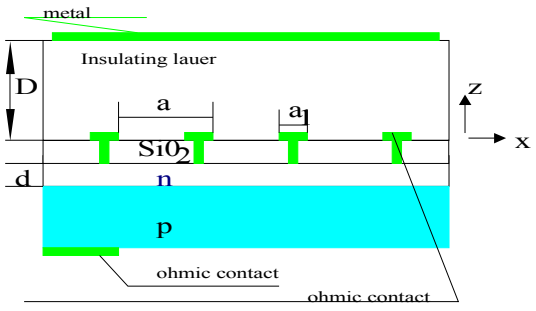


Fig.4.2 The VCC device

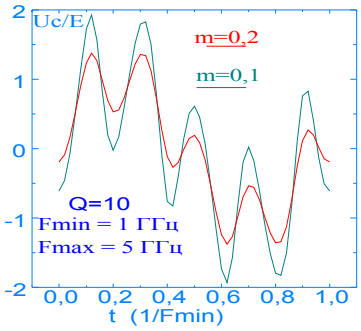


Fig. 4.3. Results of calculations

A worked example

Below an estimate is given for the parameters of VCC (cf. Fig. 4.2) to be used as a frequency converter from F_{min}= 1 GHz to F_{max} =5 GHz with 200 W peak power delivered (note, that if any of the existing varactors is used for the same purpose the power available will be *two orders of magnitude lower*).

Applied to the p-n junction is a signal with F_{max} -F_{min}=4 GHz, whereas to VCC a signal with F_{min}=1 GHz is applied, and a tuned resonance circuit with a resonance frequency F_{max} + F_{min} is used. An estimation of the basic parameters of VCC proceeds as follows:

1. Contact grid period must obey the obvious constraint

$$a < \frac{v_s}{F_{\max} + F_{\min}} = \frac{1\times10^5\, ms^{-1}}{5\times10^9\, s^{-1}} = 20\mu m$$

where ν_s is the saturated drift electron velocity in Si (=1×10^5 ms^{-1}).

2. Let the insulating layer to be fabricated from quartz (with a breakdown electric field $E \approx 10^9 Vm^{-1}$) and let a thickness of this layer to be about 100 μm.

3. The horizontal dimension of n-base (a_x) can be chosen from the condition

$$a_x = \frac{\lambda}{20} = \frac{c}{20F_{\max}\sqrt{\varepsilon}} \approx 1.5 \text{ mm}$$

the maximal capacitance being then

$$C_{\max} = \frac{2\varepsilon a_x^2}{H_d} \approx 1.5\times10^{-12} \quad \text{F}$$

4. The doping level of n-base can be varied in a wide range. Let us choose the thickness of n-base to be 1 μm with doping level of $n=5\times10^{15}$ cm^{-3}.

5. To find a maximum voltage to be applied to VCC and a minimal value of the capacitance (C_P) to be switched in parallel with p-n junction, let us assume that a fraction of voltage, which drops on p-n junction, is 1 V. Then,

$$U_c = \frac{2PQ}{F_{\min}\sqrt{0.5C_{\max}}} \approx 1000 \quad \text{V}$$

and for Q=10, P=200 W one finally obtains

$$C_{\mathrm{P}} = \frac{0.5 C_{\max} \times U_c}{1\ V} = 7.5 \times 10^{-10}\ \mathrm{F}$$

In this way, all relevant parameters of VCC are now estimated. Fig.4.3 shows the calculated time dependence of the voltage on VCC (with parameters given above) for different modulation coefficients (in the figure E is the amplitude of the lower frequency signal and m is the modulation coefficient). **More details about operational principles of VCC and some experimental results can be found in Appendix 4**